TOWARDS HIGHLY EFFICIENT MONOLITHIC DC/DC CONVERTER

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Introduction

- Types of switching regulators
  - Buck converter
  - Modes of operation of buck converter
  - Boost converter
- Structure of monolithic converter
- Method of operation of various parts of the converter.
- Integration of inductor on chip
- Integration of capacitor on chip
- Power losses in the converter
- Power flow analysis
- Issues in monolithic DC/DC converter
- Techniques to improve performance
  - Compensated error amplifier
  - Light load efficiency

Towards Highly Efficient Monolithic DC/DC Converter
What is DC/DC Converter?

- A device that accepts a DC input voltage
- Produces a DC output voltage
- Used to provide:
  - Noise isolation
  - Power bus regulation etc.
  - Output at different voltage level
  - Wide input voltage range
  - Constant output voltage
  - Galvanic isolation
Linear Regulator

- Extremely inefficient (depending on voltage drop!)
- High heat dissipation
- Bulky and expensive heat sink
- Impossible for SOC design
- Reduce battery life
- No switching noise

TOWARDS HIGHLY EFFICIENT MONOLITHIC DC/DC CONVERTER
Switching Regulator

- Takes small chunk of energy from i/p & transfer to the o/p
- Uses electrical switch & controller to regulate rate of energy
- High efficiency
- Used in portable devices- cell phones, laptops, robots, etc.
- Smaller size
- Lower heat generation
- Suitable for on chip design

Disadvantages of Switching Regulator

- Complex system design
- High frequency electrical noise
- Ripple voltage at switching frequency

Fig. Buck converter.
Types of Switch Mode Regulators

- Buck converter- step-down converter
- Boost converter- Step-up converter
- Cuk converter
- Isolated converters:
  - Flyback converter
  - Forward converter
  - Full- / Half bridge converter

Towards Highly Efficient Monolithic DC/DC Converter
Buck Converter

When Transistor ‘ON’
- Inductor current rises

When Transistor ‘OFF’
- Current through inductor passes through the diode

Modes of operation:
- Continuous mode
- Transition between continuous & discontinuous mode
- Discontinuous mode

Fig. Circuit layout of buck converter.
Continuous Mode

Now, \( V_x - V_o = L \frac{di}{dt} \)

The change in current satisfies,

\[
di = \int_{ON} (V_x - V_o) \, dt + \int_{OFF} (V_x - V_o) \, dt
\]

For steady state operation,

\[
di = 0 = \int_{ON} (V_x - V_o) \, dt + \int_{OFF} (V_x - V_o) \, dt
\]

Hence,

\[
\frac{V_o}{V_{in}} = \frac{ton}{T}
\]
**Buck Converter**

**Transition b/w Continuous & Discontinuous Mode**

- Inductor current just goes to zero.

Now, during the ON time $V_{in} - V_{out}$ is across the inductor thus,

$$I_L(peak) = (V_{in} - V_{out}) \frac{t_{ON}}{L}$$

The average current which must match the output current satisfies,

$$I_L(average \ at \ transition) = \frac{I_L(peak)}{2} = (V_{in} - V_{out}) \frac{dT}{2L}$$

$$= I_{out}(transition)$$

Where, duty ratio, $$d = \frac{t_{ON}}{T}$$

the output current at the transition point satisfies,

$$I_{out}(transition) = V_{in} \frac{(1 - d)d}{2L} T$$

**Towards Highly Efficient Monolithic DC/DC Converter**
**Buck Converter**

**Discontinuous Mode**
- Transistor OFF time divided into:
  - segments of diode conduction $d_d T$ and
  - zero conduction $d_o T$.
- The inductor average voltage gives,
  \[
  \frac{V_{out}}{V_{in}} = \frac{d}{d + \delta_d} \quad \text{---(1)}
  \]
- To resolve the value of consider the output current,
  \[
  I_{out} = \frac{I_L(\text{peak})}{2d + \delta_d}
  \]
- The change of current during the diode conduction time,
  \[
  I_L(\text{peak}) = \frac{V_o(\delta_d T)}{L}
  \]
- Thus, from above equation
  \[
  I_{out} = \frac{V_o \delta_d T (d + \delta_d)}{2L}
  \]
- Using the relationship in (1),
  \[
  I_{out} = \frac{V_{in} d \delta_d T}{2L}
  \]
Buck Converter

**Discontinuous Mode**
- Solving for the diode conduction, \( \delta_d = \frac{2L I_{out}}{V_{in} d T} \)
- The output voltage is thus given as,

\[
\frac{V_{out}}{V_{in}} = \frac{d^2}{d^2 + \left(\frac{2L I_{out}}{V_{in} T}\right)}
\]
- defining \( k^* = \frac{2L}{V_{in} T} \),

**Output voltage vs. Current**
- High O/p current voltage ratio depends on the duty ratio "d".
- Low currents discontinuous operation tends to increase o/p voltage of the converter towards \( V_{in} \).

Fig. Output voltage vs. current.

Towards Highly Efficient Monolithic DC/DC Converter
Boost Converter

- **When Transistor “ON”**
  \[ V_x = 0 \]

- **When Transistor “OFF”**
  \[ V_x = V_o \]

- **For Steady State**
  - Voltage across the inductor & average must be zero for the average current.
    \[ Vin \ t_{on} + (Vin - V_o) t_{off} = 0 \]

  - This can be rearranged to give,
    \[ \frac{V_o}{Vin} = \frac{T}{t_{off}} = \frac{1}{(1 - D)} \]

- Since, the duty ratio "D" is b/w 0 and 1 ➡️ The output voltage must always be higher than the input voltage in magnitude.

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**Fig. Boost converter circuit.**
When Transistor “ON”
- \( V_x = V_{in} \)

When Transistor “OFF”
- \( V_x = V_o \)

For Steady State
- Voltage across the inductor & average must be zero for the average current.
  \[ V_{in} \cdot t_{ON} + V_o \cdot t_{OFF} = 0 \]

- This can be arranged to give voltage ration as,
  \[ \frac{V_o}{V_{in}} = \frac{D}{(1 - D)} \]

Since, the duty ratio "D" is between 0 and 1  ➡️ The output voltage may be higher or lower than the input voltage in magnitude.

Fig. Buck-Boost Converter Circuit.
Comparison Of Different Converters

- Only the buck converter shows a linear relationship.
- The buck-boost can reduce or increase the voltage ratio with unit gain for a duty ratio of 50%.

- **Buck converter:**\[ \frac{V_o}{V_{in}} = \frac{ton}{T} \]
- **Boost converter:**\[ \frac{V_o}{V_{in}} = \frac{T}{t_{off}} = \frac{1}{(1 - D)} \]
- **Buck-boost converter:**\[ \frac{V_o}{V_{in}} = -\frac{D}{(1 - D)} \]

Fig. Comparison of voltage ratio.
Monolithic Integrated DC/DC Converters

Why Monolithic DC/DC Converter?
- Required for portable devices—laptops, mobiles etc.
- Decrease the size & weight of these devices.
- Miniaturization of the power modules.
- Integrating a DC-DC converter can potentially lower the parasitic losses as interconnect b/w DC-DC converter & microprocessor is reduced.
  - Need for on chip, point-of-load (PoL) power conversion.

Challenges
- Tight area constraint for the on-chip integration of inductive & capacitive elements.
- Poor parasitic impedance characteristics.
- High frequency ➔ low value & physical size of passive devices required.
Applications

- Battery operated portable electronic devices like laptops, cell phones, PDAs (Personal digital assistants) & other palm devices.

Fig. Laptop computer power supply system.
Monolithic Integrated DC/DC Converters

**Components**
- Power stage
- Compensator
- Modulator
- Voltage to current converter
  - Sensed inductor signal
  - Ramp signal
- Oscillator & ramp generator
- Pulse width generator
- Buffer

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Fig. Structure of a current mode buck converter.
Power stage: Inductors for On Chip DC/DC Converter (MHz Frequency)

- MEMS based inductors.
- Use iron-based alloy plated on Si substrate.
- Is a metal slab completely encapsulated by a magnetic material.
- Spirals made of 1μm Al-Cu isolated from ground plane by 0.5 μm of SiO₂.
- The magnetic film surrounding metal is amorphous CoZrTa alloy that exhibits:
  - Small hysteresis losses.
  - Withstand temperature up to 450 °C.
  - Integrated in standard high temperature CMOS Si process.
  - Cut off frequency of approx. 1.4GHz.
- Superior higher frequency & saturation characteristics.
- Reduces size & parasitic effects.
- Performs at frequency up to & beyond 10 MHz.
- Magnetic material below & above spirals prevent straying of magnetic flux.
- One layer of magnetic material increases inductance by 36-50% & two layers by 100-500%.

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Power stage: Inductors for On Chip DC/DC Converter (MHz Frequency)

- CoHfTaPd – Co based amorphous alloy can also be used at high frequency (few MHz).

**Fig. Cross sectional view of monolithic DC-DC converter.**

**Fig. Top view of monolithic DC-DC converter. Size of inductor (4mm* 4mm)**

**Fig. Circuit model of single layer spiral circuit.**
Limited area overhead. Filter capacitance integrated on a microprocessor is limited.

Ranges between 100nF – 1nF.

As capacitance decreases, filter inductance & switching frequency both increase to satisfy output voltage & current.

Switching & conduction power dissipation of power MOSFETS & filter inductor increases.

Efficiency degrades.
**Cascode OTA (Operational Trans-conductance Amplifier)**

for Power stage of current mode converter

- Control-to-o/p transfer function has real poles.
- Pole from o/p filtering capacitor heavily dependent on equivalent resistance of load $R_L$.
- Poor frequency response.

➢ **Dynamic Response** ➢ **Pole-Zero Cancellation Preferred.**

- Band width can be extended.
- Speed up response time

Transfer function of Compensator is:-

$$A(s) = \frac{V_a}{bV_o} \approx g_m R_o \frac{1 + sC_C R_Z}{1 + sC_C R_o}$$

, for $R_o >> R_Z$.

where, $g_m$ ➔ Trans-conductance of OTA

$R_o$ ➔ O/p resistance of the OTA.
Compensator

- $g_m$ & $R_o$  → Important for frequency compensation.
  → Determine gain & phase margin of DC/DC converter.
  → Depend on biasing current.

Result

- Average -20 dB/dec closed loop-gain.
- Sufficient phase margin below unity gain frequency.
- Two Stage OTA  → Higher gain
  → Large output swing.
Cascode OTA (Operational Trans-conductance Amplifier)

Circuit Implementation

 ✓ Single stage amplifier.
 ✓ High gain & only one dominant pole.

Fig. Schematic of the Cascode OTA.
On Chip Current Sensing Technique (to Sense Inductor Signal)

- Aspect ratio of $M_2 \ll M_1$ in power stage.
- Op amp enforce same voltage at node A & B.
- O/p current $I_O$ flows through $M_1$.
- Switch MS$_1$ is shorted.
- $V_{DS} (M_1) = V_{DS} (M_2)$.
- $I_S$ (Sensing current) $\ll I_O$.
- $I_2 \ll I_S$.
- $V_{sense}$ in control feedback loop.
- $M_{RS}$ operate in saturation.

The sensing scheme needs to be realized with high bandwidth & low power consumption.

Fig. Schematic of on chip current sensing circuit.
On Chip Current Sensing Technique (to Sense Inductor Signal)

Characteristics

- \[ V_{\text{sense}} = I_{\text{sense}} R_{\text{sense}} = I_L R_{\text{sense}} / 1000 \]
- High gain amplifier required for accurate current sensing.

- Accuracy of sensed current depend on:
  - current mirror \( M_1 \) & \( M_2 \).
  - On-chip resistor \( R_{\text{sense}} \).

- Matching of \( M_1 \) & \( M_2 \) depend on:
  - Mobility, \( \mu \).
  - Oxide capacitance, \( C_{\text{ox}} \).
  - Threshold voltage, \( V_T \).
  - Location of \( M_2 \) to minimize error.

Fig. Schematic of on Chip Current Sensing Circuit.
Advantages

- $I_{\text{sense}}$ small
  - Hence, power loss reduced in the sensing circuit.
  - Improve efficiency of converter.

On-chip current-sensing circuit can be extended to sense power NMOS transistor by building complementary circuit for other topologies – boost converter & buck-boost converter.

Fig. Schematic of on Chip Current Sensing Circuit.
Comparator

- Needed in both:
  - modulator in feedback control (PWM control).
  - hysteretic comparator in the Oscillator & ramp generator circuit.

- Implemented by a source-coupled differential pair with positive feedback to provide a high gain.

- Gain of positive feedback gain stage is:

\[
A_v = \frac{\mu_p \left( \frac{W}{L} \right)_1}{\mu_n \left( \frac{W}{L} \right)_3} \cdot \frac{1}{(1 - \alpha)}
\]

where, \( \alpha = \frac{W}{\left( \frac{W}{L} \right)_3} \) is the positive feedback factor.
Use of Inverter Chains

- Inverter chains \( M_{12} - M_{15} \).
- Increase the response of comparator o/p signal.
- Act as driver stage such that:
  - \( M_7 \) & \( M_8 \) can be made smaller.
  - Reduce parasitic capacitance at gates of \( M_7 \) & \( M_8 \).
  - Results Faster Response.

Fig. Schematic of the Comparator.

Simulation: 15ns delay time Adequate for applications with switching frequency of few MHz.
Oscillator and Ramp Generator

- **Used to generate:**
  - The clock & ramp signals for PWM control.
  - Compensation slope for current mode converter.

- **Consists of:**
  - Voltage-to-current (V-I) converter.
  - Hysteretic comparator.

- **Clock frequency & slope of compensation ramp are:**
  - Synchronized with each other.
  - Depend on \( V_{\text{ref}}, C_t, R_t, V_H \) & \( V_L \).

\( R_t \) & \( C_t \) can be off-chip components → Switching frequency can be adjusted for different applications.

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V-I Converter

- In current mode converters, compensation ramp add with inductor current signal to avoid sub harmonic oscillations.
- V-I designed to convert ramp signal & sensing inductor signal into current.
- V-I converter is a cascade of:
  - Source follower
  - Common-source config.
  - I/p voltage of ramp vol. & sensing voltage range from 300-1000mV.
  - Not high enough to turn ‘ON’ M₂ & M₄.

Fig. Schematic of the V – I converter.
Now, $V_A = V_{in} + V_{SG1}$

For 2\textsuperscript{nd} stage V-I converter:

Trans-conductance,

$$g_m = \frac{L_1}{V_A} = \frac{g_{m2}}{1 + g_{m2} R_S} \approx \frac{1}{R_S} \text{ for } g_{m2} R_S \gg 1$$

Then, the o/p current is given by,

$$I_1 = \frac{V_A}{R_S} = \frac{V_{in} + V_{SG1}}{R_S}$$

Need to eliminate non-ideal term, $\frac{V_{SG1}}{R_S}$

Now, $I_2 = \frac{V_{SG3}}{R_S}$

Hence, o/p current $I_{out}$,

$$I_{out} = I_1 - I_2 = \left( \frac{V_{in}}{R_S} + \frac{V_{SG3}}{R_S} \right) - \frac{V_{SG1}}{R_S} = \frac{V_{in}}{R_S} \alpha V_{in}$$

Fig. Schematic of the V – I converter.
Now, sensing voltage, \( V_{\text{sense}} = I_{\text{sense}} R_{\text{sense}} \).

Hence, o/p current, \( I_{\text{out}} \) do not depend on value of \( R_s \) & \( R_{\text{sense}} \), rather on the ratio.

- Can be easily controlled.

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**V-I Converter**

Fig. Schematic of the V – I converter.
Pulse width Generator

- S=1, R=1 is a forbidden state for the SR latch.
- At startup, O/p of compensator $V_c$ is low compared with sum of the ramp & sensed signal.
- Hence, R is always high.
- However, the given circuit ensures that RS latch do not reach forbidden state.
- R & S do not go high simultaneously.

Fig. Schematic of Pulse width Generator.
Buffer

- Required for receiving and amplifying the signal produced by the control circuit.
- Poorly designed buffer with a simple inverter Chain a shoot-through current will occur and a large current will pass through the power transistors during each switching transition.
- Hence, buffer without short-circuit power consumption is needed.
- Power rails of the buffer should be laid-out carefully & resistances to be minimized so that the converter efficiency do not degrade.

TOWARDS HIGHLY EFFICIENT MONOLITHIC DC/DC CONVERTER

Fig. Schematic of buffer without short-circuit power consumption.
Power Losses in DC/DC Converter

- **Conduction Loss**
  - Related to the size of Power Transistors
- **Switching Loss**
  - Optimum Sizing required to improve Efficiency.
- **Shoot through current Loss**
  - Related to design of buffer Stage to drive power transistors.

Significant energy dissipated in parasitic impedances of circuit board inter connect & discrete components of the regulator.

- **Conduction Losses**: Caused by the parasitic resistive impedances.
- **Switching Losses**: Due to parasitic capacitive impedances of circuit components.
- Power consumed by PWM feedback circuit & integrated filter capacitor is small as compared to the power consumption of the power train (the power MOSFETs, MOSFET gate drivers, the filter inductor).
Buck converter O/p, \( V_{DD2}(t) = DV_{DD1} + V_{\text{ripple}}(t) \).  

Ripple Current, \( \Delta i = (V_{DD1} - V_{DD2})D/2Lf_s \). 

Amplitude of voltage ripple,

\[
\Delta V_{DD2} = \frac{(V_{DD1} - V_{DD2})D}{16LCf_s^2} = \frac{\Delta i}{8Cf_s}
\]

where, \( L \) — Filter inductance.  
\( C \) — Filter Capacitor.  
\( f_s \) — Switching frequency.
**MOSEFETs Related Power**
- Combination of conduction loss & dynamic switching loss.
- Conduction power: Dissipated in series resistance of transistor.
- Dynamic Power: Dissipated in each switching cycle of charging/discharging of gate oxide, gate-to-source/drain overlap & drain-to-body junction capacitance of MOSFET.
- MOSFET width optimized to minimize power dissipation.
- Optimized power consumption:

\[
P_{\text{tot,MOS}(\text{opt})} = a \sqrt{\left(1^2 + \frac{i^2}{3}\right) f_s}
\]

\[
a = 2(\sqrt{R_{\text{ONMOS}}(1 - D)E_{\text{NMOS}}} + \sqrt{R_{\text{OPMOS}}DE_{\text{PMOS}}})
\]

\[
E = 2(C_{\text{ox}} + C_{\text{gs}} + 2C_{\text{gd}} + C_{\text{db}})V_{DD1}^2
\]

Where, 
- \(R_o\) equivalent series resistance of a 1\(\mu\)m wide transistor.
- \(C_{\text{ox}}\) gate oxide capacitance.
- \(C_{\text{gs}}\) gate-to-source overlap.
- \(C_{\text{gd}}\) gate-to-drain overlap.
- \(C_{\text{db}}\) drain-to-body junction capacitance.
Filter Inductor Power

Energy consumption due to:
- Series resistance of filter inductor.
- Stray capacitance of filter inductor.

Total power consumption in inductor is:

\[
p_{\text{tot, inductor}} = b\left(\frac{l^2}{\Delta i f_s} + \frac{\Delta i}{3 f_s} + \frac{C_{Lo} V_{DD1}^2}{R_{Lo} \Delta i}\right)
\]

\[
b = \frac{(V_{DD1} - V_{DD2}) D R_{Lo}}{2}
\]

Where,
- \(C_{Lo}\) → Parasitic stray capacitance per nH inductance.
- \(R_{Lo}\) → Parasitic series resistance per nH inductance.
Filter Capacitor Related Power

Integrated Capacitor implemented utilizing Gate Oxide Capacitance of MOSFET

Total Power dissipation of a filter Capacitor is:

\[ P_{\text{tot, capacitor}} = d f_s \Delta i \]

\[ d = \frac{8 R_{\text{ocap}} L_{\text{cap}} C_o \Delta V_{DD2}}{3} \]

Where,
- \( R_{\text{ocap}} \) → Series capacitance of MOSFET with 1\( \mu \)m width.
- \( C_o \) → Gate oxide capacitance per \( \mu \)m\(^2\).
- \( L_{\text{cap}} \) → Channel length of the MOSFET.
Total Power Consumption of Buck Converter

\[ P_{buck} = P_{\text{tot,MOS (opt)}} + P_{\text{tot,inductor}} + P_{\text{tot,capacitor}} \]

\[ P_{buck} = a \sqrt{(I^2 + \frac{i^2}{3})} f_s + b \left( \frac{l^2}{\Delta i f_s} + \frac{\Delta i}{3f_s} + \frac{C_{lo} V_{DDL}^2}{R_{Lo} \Delta i} \right) + d f_s \Delta i \]

- Strongly function of switching frequency \((f_s)\) & ripple Current \((\Delta i)\).
- \(P_{\text{tot, capacitor}}\) \(\uparrow\) As \(f_s\) & \(\Delta i\) \(\uparrow\).
- \(P_{\text{tot, inductor}}\) \(\downarrow\) As \(f_s\) & \(\Delta i\) \(\downarrow\).
- \(P_{\text{tot, capacitor}}\) Negligibly small (less than 1%) as compared to inductor & MOSFET power.
Efficiency Analysis in DC/DC Converter

- **Efficiency**, $\eta = 100 \times \frac{P_{\text{Load}}}{P_{\text{Load}} + P_{\text{buck}}}$

$$P_{\text{buck}} = a \sqrt{(l^2 + \frac{i^2}{3}) f_s + b \left( \frac{l^2}{\Delta i f_s} + \frac{\Delta i}{3 f_s} + \frac{C_{\text{Lo}}V_{\text{DD}}^2}{R_{\text{Lo}} \Delta i} \right) + df_s \Delta i}$$

- Low $f_s$ & $\Delta i$ → Power dissipation mainly in the Inductor.
- As $f_s$ & $\Delta i$ (↑) → Inductor Loss (↓)
  Parasitic Loss (↓)
  MOSFET Power Loss (↑)
- As Inductor loss dominate → Loss (↓)

Fig. (a) MOSFET power (b) inductor power (c) capacitor power as functions of $\Delta i$ & $f_s$.

$\Delta i$ in Amps & $f_s$ in MHz.
As the filter capacitance decreases, the filter inductance and switching frequency are both increased to satisfy the output voltage and current requirements. Both the switching and conduction power dissipation of the power MOSFETs and the filter inductor increases, thereby degrading the efficiency.

Major challenges for a monolithic switching DC-DC converter:
- The area occupied by the integrated filter capacitor.
- The effect of the parasitic impedance characteristics of the integrated inductors on the overall efficiency characteristics of a switching DC-DC converter.
Battery-powered portable electronic devices like cell phones, laptops, etc.

- Full loading not present for prolonged periods.
- Rather devices run at light loads (stand-by mode) for most of the time.

**Region I**
- Conduction losses dominate.

**Region II**
- Switching losses proportional to load current, i/p voltage, switching frequency.

**Region III**
- Gate-drive losses while charging / discharging gate capacitances of power transistors during switching transition.

**Fig. Efficiency curve of DC/DC converter.**

*Decreasing Switching Frequency ➔ Best way to Reduce Total Loss.*
Compensated Error Amplifier (for Fast Transient Response)

- Fast transient response of o/p voltage reveals critical point for large load variations.
- Required to supply reliable voltage.

**Solution**
- Large transconductance for the error amplifier for large load variations.
- Uses on-chip current mode Miller capacitor (replaces large Off capacitor).
- Decrease transient response time.
Compensated Error Amplifier (for Fast Transient Response)

Fig. Timing analysis of signal waveforms. (a) With a positive & sudden load variation. (b) With a negative & sudden load current variation.
Compensated Error Amplifier (for Fast Transient Response)

- Better Response Time.

Fig. The transient response with load current step b/w 100mA & 400mA.
(a) Conventional error amplifier. (b) On-chip compensated error amplifier without fast transient controller. (c) On-chip compensated error amplifier with fast transient controller.
Issues with Monolithic DC/DC Converters

- High efficiency with large input voltage range.
- High performance system-on-chip (SOC) systems.
- Dynamic power management.
- Fast dynamic response.
- Low power consumption: low stand by power.
- Need to provide robust output voltage regulation.
- Maximum efficiency.
- Minimize ripple noise on input & output.
- Minimize cost.
- To have accurate sensed current for current mode PWM controller.
- Reduce supply voltage demand, greater amount of current from external power supplies.
- Voltage scaling capability.
Books


Research Papers


Questions???

THANK YOU !!!