Dynamic Random Access Memory (DRAM)

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Outline

- Classification
- DRAM Overview
- Soft Errors
- Design Consideration & Capacitor Layout
- Types of DRAM
- Market Trends
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Classifications

- Memory vs Combinatorial Circuit
- Dynamic vs Static
- Random Access
- Volatile vs Non-Volatile
- Read-Only vs Read-Write
Memory

- Output reflects whatever have been stored
- Most of the memory element have two states
- We call them ‘1’ and ‘0’
- States might be charge, bistablity, magnetic coupling, fuses

- Combinatorial Circuit
  - Output is purely a function of input
Static and Dynamic Circuits

- Output is connected to a low impedance node
- Output is capable of driving loads
- Output is connected to a high impedance node, a capacitor
Volatile and Non-Volatile Memories

- Memory element looses its content if power supply is switched off
  - DRAM, SRAM
- Power supply is not needed to maintain the stored information
  - ROM, PROM, EEPROM, magnetic & optical storage
Random Access

- Any piece of data can be accessed in nearly the same time, irrespective of its physical location or previous data

- RAM, ROM, EEPROM are Random Access types

- Magnetic and optical memories are not Random Access
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DRAM Cell - 1 transistor cell

- 1: capacitor is charged
  0: capacitor is discharged

- **Write**
  - Wordline -> high
  - Bit-line -> high / low

- **Read**
  - Precharge Bit-line
  - Wordline -> high
  - Probe Bit-line
  - Destructive – so cell content is re-written
**DRAM Cell - 1 transistor cell**

- **Refresh**
  - Charge in storage capacitor eventually leaks off due to finite leakage current
  - So refresh is needed
  - In most cases, it is done periodically every 5-10ms
  - Different schemes available
    - Distributed
    - Burst
Chip Organization

- Row Decoder selects a Row
- Column decoder read/write bits of that row
- Sense Amp read, refresh
- Bit-line can be very long

DRAM (Dynamic Random Access Memory)
Sensing

- $V_{storage}$ is close to 0 and $V_{dd}$
- $V_{pre}$ is Pre-charge voltage is kept close to $V_{dd}/2$
- $C_s \sim 40 fF$
- $C_{BL} \sim 30x$ larger than $C_s$
- $\Delta V \sim 100 mV$

$$\Delta V = \left(V_{Stored} - V_{pre}\right) \frac{C_s}{C_s + C_{BL}}$$
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Soft Errors

- High energy particle strikes the device
  - Strikes releases electron and hole pairs
  - These charges can be absorbed by source and drain and change state of device

- Soft Errors don’t cause permanent damage to the hardware, but can alter the data
Origin

- Packaging of the device
  - It is usually contaminated with radioactive materials like Uranium ($^{238}$U), Thorium ($^{232}$Th), Polonium ($^{210}$Po)
  - Generate $\alpha$-particles
  - Confirmed by IBM in 1984

- Cosmic Rays from deep space
  - Strikes by high energy neutron and proton cause soft errors
  - Neutron flux is higher in higher altitudes
  - Confirmed by Intel in 1978
Critical Charge: $Q_{\text{crit}}$

- $Q_{\text{crit}}$ of a circuit is minimum charge deposited by a particle to cause malfunctioning of the circuit.
- If induced charge is same as charge stored in the DRAM cell then state may get flipped.
- Increasing the stored charge on the DRAM storage capacitor increases $Q_{\text{crit}}$ hence decreases SER.
- If strike is on the sensitive node of SRAM, generated current pulses can propagate and causing state transition.
Stopping Power

- The energy lost per unit track from interaction of high energy particle and silicon crystal

- This energy provides the required energy to generate electron-hole pairs

- $\alpha$-particle with 10MeV energy has stopping power of 100keV / $\mu$m
What an α-Particle can do

- **Assuming**
  - Capacitance: 2fF/µm
  - Supply Voltage: 1.2V
  - α-particle: 10MeV, 100keV/µm
  - Energy required to produce 1 pair: 3.6eV

- **Solution**
  - Total Charge in cell = 2x1.2 = 2.4fC / µm
  - No. of electron-hole pairs generated = 100k / 3.6 = 2.8x10^4 /µm
  - Total Charge generated = 2.8x10^4x1.6x10^{-19} = 4.5 fC/µm

4.5fC/µm > 2.4fC/µm => this can upset the cell
DRAM Requires...

- A very low leakage current
- Sufficient storage capacitance,
  - so that voltage change at bit-line can be sensed by sense amp
  - Q-critical is sufficiently large
- Less sensitive to alpha particles, which causes soft errors
- Low series resistance (R) and capacitance (C)
- All this in ever decreasing cell area
How good are DRAMs?

- High density and low cost per bit, cell is nearly ten times smaller than SRAM cell
- However SRAM offers lower power consumption and high performance
- Low error tolerance
- Need refresh – greatest disadvantage
- Can be embedded along with processor
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Design Consideration for Electronics

- Speed
- Power
- Errors

DRAM (Dynamic Random Access Memory)
Density – Memory Chips

- Density
- Speed
- Power
- Errors

DRAM (Dynamic Random Access Memory)
Design Perspective

- Decoders
- Sense Amplifiers
- Access Transistor
- Storage Capacitors
  - Planar
  - Trench Capacitor
  - Stacked Capacitor
Decoders

- NOR Decoder uses pseudo-nMOS NOR logic
  - # of transistors used are large $O(N \cdot 2^N)$ for $N$ addresses
  - Less delay

- Tree Decoder
  - Very few transistors $O(2^N)$ for $N$ addresses
  - High density
  - Huge delay due to many transistors in series

Source: Microelectronics Circuits, fifth edition, by Adel S. Sedra and Kenneth C. Smith
Sense Amplifier

- Presence of noise sources
  - Transients, Radiation induced charge
  - Coupling of switching disturbances
  - Sense amplifier $V_t$ mismatch

- An example of differential sense amplifier with positive feedback
  - Assumes the presence of Bit-Line and its complement for all cells

Source: Microelectronics Circuits, fifth edition, by Adel S. Sedra and Kenneth C. Smith
Access Transistor...

- **Resistance**
  - Channel ON resistance of the MOSFET
  - Due to bit-line contact

- If \( V_{dd} \) is the supply voltage
  - At max \( V_{dd} - V_t \) can be stored
  - \( V_t \) increases as drain-source voltage decreases
  - And also due to Body Effect

\[
i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t)^2
\]

\[
i_D = \mu_n C_{ox} \frac{W}{L} \left[ (v_{GS} - V_t)v_{DS} - \frac{1}{2} v_{DS}^2 \right]
\]

\[
V_t = V_{t0} + \gamma \left[ \sqrt{2\Phi_f + V_{SB}} - \sqrt{2\Phi_f} \right]
\]

Where
- \( V_{t0} \) is the threshold voltage for \( V_{SB} = 0 \)
- \( \Phi_f \) is a physical parameter with \( (2 \Phi_f) \sim 0.6V \)
- \( \gamma \) is a fabrication-process parameter

DRAM (Dynamic Random Access Memory)
Access Transistor

Scaling Issue
- Decrease in pitch of word-lines (to increase density)...
- Decrease in channel length L...
- Decrease in oxide thickness (t_{ox}) due scaling rules...
- Decrease in gate-to-source voltage...
- Decrease in Charge in Storage Capacitor...
- Decrease in sensing time...

Low $V_t$ MOSFET
- If $V_t$ is low, supply voltage can be scaled down
- $V_{\text{WLL (word-line-low)}}$ can be allowed to be negative to fully turn OFF the device
Storage Capacitor...

- $C_s$ (Storage Capacitance) = $A k \varepsilon_0 / t_{ox}$

- $t_{ox}$: Oxide thickness
  - Use of thin dielectric, while limiting the leakage current.

- $k \varepsilon_0$: Dielectric Constant
  - Use of insulating material with higher dielectric constant
  - $\text{SiO}_2$ ($k=3.9$) $\rightarrow$ $t_{ox} \sim 3\text{nm}$
  - $\text{ONO}$ ($k=7$) $\rightarrow$ $\sim 2.5\text{nm}$ (nitride oxide composite)
  - $\text{Ta}_2\text{O}_5$ ($k\sim30$) (Tantalum pentoxide)

Source: [http://www.doitpoms.ac.uk/tlplib/dielectrics/capacitors.php](http://www.doitpoms.ac.uk/tlplib/dielectrics/capacitors.php)
...Storage Capacitor

- A: Area, different layouts have been tried out
  - A 3-D capacitor structure
  - Parasitic, Planar, Trench, Stacked, Crown

- Series resistance
  - Connection between MOSFET & capacitor
  - Parasitic resistance of capacitor itself.
  - R < 50kΩ

Source: http://www.doitpoms.ac.uk/tlplib/dielectrics/capacitors.php
Capacitor Layout

Source: “Prozessintegration und Bauelementearchitekturen (LEB)” Lecture Notes, Prof. Ryssel
Planar Capacitor

- Occupies a large surface area as compared to a transistor

Source: http://patimg2.uspto.gov
Trench Capacitor

- Planar chip possible
- Embedded DRAM
- Not compatible with high-\(\varepsilon\)-films, material may not survive if transistor is simultaneously processed
- Increasingly high aspect ratio of trench are difficult to etch
- Decouple effective surface area of capacitor with area of array cell

Source: “Prozessintegration und Bauelementearchitekturen (LEB)” Lecture Notes, Prof. Ryssel
Trench Fabrication Process

Source: "Prozessintegration und Bauelementearchitekturen (LEB)" Lecture Notes, Prof. Ryssel
Stack Capacitor

- Surface area considerably less than trench capacitor
- Taller Structures causes mechanical instability problems
- Difficult to wire over the topography of such tall capacitor
- Compatible with high-\(\epsilon\)-film

Figure 3
Schematic cross section of stacked capacitor cell suitable for 0.15 \( \mu \)m.
Area Enhancement Technique

minimum feature size: (a) Resist recess for SiN barrier definition in lower portion of trench; (b) LOCOS sidewall oxidation (isolation collar) after barrier etch and resist strip; (c) bottle enlargement using isotropic Si etching; (d) buried-plate formation self-aligned to the collar, node dielectric formation.


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DRAMs Types...

- **eDRAM**
  - Embedded DRAM
  - DRAM is integrated in same die or package as main ASIC or processor
  - Large amount of memory can potentially be used
  - Noise reduction

- **FPRAM**
  - Fast Page Mode DRAM
  - Row need not be selected each time new data is to be read from same row
  - Saves delay of pre-charge and accessing the row
EDO DRAM
- Extended Data Out DRAM
- A new access cycle can be started while keeping the data output of the previous cycle active

SDRAM
- Synchronous DRAM
- Traditionally DRAMs have asynchronous interface, SDRAM has synchronous
- This feature allows SDRAM to be widely used in computers
...DRAMs Types

- DDR SDRAM
  - Double Data-Rate Synchronous DRAM
  - Double Data Rate uses both rising and falling edge of the clock.
  - DDR1, DDR2, DDR3 increase in number of stages of the pipelining, increase in latency, increase in overall speed, e.g. DDR2 employs an I/O buffer between the memory and data-bus so as to further double the frequency.
  - Present PCs have DDR2 SDRAM, DDR3 SDRAMs are also available
  - $2 \times 2 \times 64/8 = 32$ bytes transfer per memory clock cycle
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History

- In 1966 DRAM was invented by Dr. Robert Dennard at the IBM Thomas Research Center and he was awarded U.S. patent in 1968
- Intel 1103 was first commercially available DRAM-memory in 1970
- The first DRAM with multiplexed row and column address lines was the Mostek MK4096 (4096x1) designed by Robert Proebsting and introduced in 1973
- At the 16K density the cost advantage increased, and the Mostek MK4116 16K DRAM achieved greater than 75% worldwide DRAM market share
Market Trends - Memory

Semiconductor memory market as a percentage of total IC market

- Semiconductor memory market accounts for almost one-third of total IC market

Source: Introduction to advance semiconductor memories
Market Trends - DRAM

Comparison of different MOS memory share

- DRAMs are currently (and predicted to be in the future) the largest memory segment in terms of dollars sales.

- Flash memories growing at much faster pace.

Source: Introduction to advance semiconductor memories.
Most of the company have been researching Barium-Strontium-Titanate (BST) as the most likely candidate for the dielectric material
\[ (Ba_xSr_{1-x})Ti_{1+y}O_{3+z} \quad (k = 200-400) \]

Thyristor based SRAM cell called T-RAM – with cell area 1/10\(^{th}\) of conventional SRAM cell

Suitable packaging material / radiation hardening to make chip insensitive to Soft Errors

DDR4 SDRAMs expected to come into the market in 2012, expected to run at 1.2V and clock speed of 1600MHz

Multilevel (ML) storage, which refers to storage of more than 1bit per cell
References

- “Prozessintegration und Bauelementearchitekturen (LEB)” Lecture Notes, Prof. Ryssel
- Tutorial on Architecture Design for Soft Errors, Copyright(c) Emer & Mukherjee
Thank You