HIGH EFFICIENCY MONOLITHIC DC-DC CONVERTERS

Presented By-
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HIGH EFFICIENCY MONOLITHIC DC-DC CONVERTERS - OUTLINE

- Background
- Advantages and difficulties in integrating converters
- Descriptions of some on-chip implementations
  - Linear regulators
  - On-chip controllers for PWM, feedback etc.
  - Switched capacitor circuits
  - Hybrid regulators
  - Cascode-bridge circuits
- Integration of passive components
- References
BACKGROUND

Various topologies for DC-DC converters have been developed, some of which are listed below:

1. Fundamental circuits, buck, boost and buck-boost
2. Voltage-lift and super-lift
3. Transformer type
4. Switched capacitor and switched inductor converters
5. Soft-switching i.e. ZCS-QRC, ZVS-QRC, ZTC converters
6. Synchronous rectifier converters
7. Multi-elements resonant power converters

Some of these topologies will be briefly described, focus on linear regulators, buck converters and switched capacitor circuits because of their importance to monolithic converter design.
- Fundamental Circuits:
  - Buck Converter:
    ![Buck Converter Circuit](image1)

  - Boost Converter:
    ![Boost Converter Circuit](image2)

  - Inverting Buck-Boost:
    ![Inverting Buck-Boost Circuit](image3)

  - Non-inverting:
    ![Non-inverting Circuit](image4)
Switched Capacitor Circuits –
- The advantages of switched capacitor circuits are fully-integrated design, with no off-chip passive components required. No inductor is required which saves space and eliminates EMI due to switching.
- The limitations are low efficiency because of large parasitics for on-chip capacitors and large chip area required for fabricating capacitors.

Closed-Loop/Feedback –
- Feedback mechanisms compare output voltage with a reference and set output voltage/current accordingly
- Advantage is better load regulation
- Drawback is slower transient load response due to inherent delay of the feedback controller
Linear Regulators –
  - General Idea:

  - Ideal Efficiency
    \[ \eta_{\text{max}} = \frac{V_{DD2}}{V_{DD1}}, \]

  - Define current efficiency as a parameter for evaluating circuit performance
    \[ \eta = \frac{V_{DD2}}{V_{DD1}} \eta_{\text{current}}, \]
    \[ \eta_{\text{current}} = \frac{I_{\text{out}}}{I_{\text{in}}}, \]

  - So that

  - Source – Multi-voltage CMOS Circuit Design
Transformer Type:

In this topology, a transformer is placed in between the supply and filter inductor. This achieves the double advantages of providing voltage scaling if necessary and also isolating the load from supply.

Synchronous Rectifier:

In synchronous rectifier DC-DC converters, a low-forward resistance MOSFET switch is used in place of the diode rectifier. This configuration has the advantages of allowing two-way power transfer, which is useful in case of regenerative braking, and also the conduction losses reduce resulting in improved efficiency.
Soft-switching scheme –

Full-bridge circuit with capacitive snubbers added:

Transistor T1 switching waveforms:
ADVANTAGES AND DIFFICULTIES FOR INTEGRATION

Reasons for integrating DC-DC converters on-chip –

- Reduction in converter size, volume and weight necessary for portable applications
- Increase in efficiency due to a variety of reasons (enumerate: Better and fast response to load variations, reduction in miss-match of impedances, less parasitic, interconnect loss etc.)
- High frequency operation
- Improvement in power management and regulation using multiple outputs
- Can place converter closer to load (mu-P chip) which reduces input current requirement and relaxes constraints on output impedance of source
- Conversion to lower voltages is achieved easily
ADVANTAGES AND DIFFICULTIES FOR INTEGRATION

Challenges in integrating converters –

- Integration of passive components is a key barrier for a variety of reasons (enumerate: Large chip area, lesser quality factors, higher parasitic, limitation of maximum achievable values etc.)
- Difficult to maintain overall efficiency as frequency increases
- Lack of accurate models
- Only a small amount of power can be realistically converted (< 1W) and the power density is quite high

Reference Papers (for entire section):
- Integration of a power supply for system-on-chip
- Multi-voltage CMOS Circuit Design
- DC-DC Power Converter for Monolithic Implementation
GENERAL IMPLEMENTATION ON-CHIP
1. LINEAR REGULATORS

- An example of a high efficiency linear regulator circuit:

<table>
<thead>
<tr>
<th>Mode</th>
<th>Charging Mode</th>
<th></th>
<th>Discharging Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Driving</td>
<td>3 x 1</td>
<td>2 x 1</td>
<td>1</td>
</tr>
<tr>
<td>Current</td>
<td></td>
<td></td>
<td>= 0</td>
</tr>
<tr>
<td>Circuit</td>
<td>V_DD</td>
<td>V_DD</td>
<td>V_DD</td>
</tr>
<tr>
<td>Equivalent</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_out</td>
<td>V_ref-low-3 &gt;</td>
<td>V_out</td>
<td>V_ref-high-1 &gt;</td>
</tr>
<tr>
<td></td>
<td>V_ref-low-2 &gt;</td>
<td>V_out</td>
<td>V_ref-high-2 &gt;</td>
</tr>
<tr>
<td></td>
<td>V_ref-low-1 &gt;</td>
<td>V_out</td>
<td>V_ref-high-3 &gt;</td>
</tr>
</tbody>
</table>

Source – Multi-voltage CMOS Circuit Design
- An example of a high efficiency linear regulator circuit:

- Source – Multi-voltage CMOS Circuit Design
CHIP
2. ON-CHIP SWITCHING CONTROLLERS

- Conventional implementation:
  - OPAMP integrator followed by a comparator, is limited by the bandwidth and slew rate of the OPAMP and comparator.
  - Feedback circuit, simply compare output voltage and an external reference voltage and increase output voltage if less and vice versa. This can be implemented by increasing duty-cycle in PWM type, or increasing output capacitor charging time in switched capacitor type. Feedback is also often used along with other mechanisms to improve output regulation.
Implementation of Analog-PWM –

- The PWM is a three terminal block the first input terminal is the battery voltage, the second input terminal is the reference current and the output terminal is a voltage square wave with current controlled duty cycle that control the output voltage of the converter so as the on-time increase the voltage increase and as the on-time decrease the voltage decrease. The relation between the input voltage and the output voltage is given by:

\[
D = \frac{V_o}{V_B} = \frac{I + I_{ref}}{2I}
\]

Circuit for triangular waveform:
○ Current comparator:

○ Rail-to-rail current conveyor:
Implementation of digital PWM –

- In this case, the integrator + comparator are replaced by an A/D converter followed by a digital controller. The advantages are easier on-chip implementation as compared to analog circuitry and the possibility of the controller being programmable which can then be optimized for the available external passive components. Four simple implementations for generating a digital PWM waveform will be described here.
  - Fast clocked counter type:
- Tapped delay line PWM generator:

- A hybrid version proposed in “Variable Supply-Voltage Scheme with 95%-Efficiency DC-DC Converter for MPEG-4 Codec”:
CHIP
2. ON-CHIP SWITCHING CONTROLLERS

- Switching regulator based on passive sigma-delta modulator proposed in “A Low-Power Digital PWM DC/DC Converter based on Passive Sigma-Delta Modulator”:
3. SWITCHED CAPACITOR CIRCUITS

- Voltage doubler (step-up) circuit
  - Network Circuit:
  - Actual Circuit:

- Source - switched-capacitor dc-dc converters for Low-power on-chip applications
Voltage scalable SC down converter:

- Network/topology circuit:

Source - Voltage Scalable Switched Capacitor DC-DC Converter for Ultra-Low-Power On-Chip Applications
- Actual architecture with frequency scaling:

- At low load power, when the number of $\Phi 2$ cycles reduces the frequency scaler halves frequency in order to reduce switching losses and doubles frequency when the converter cannot supply load power i.e. $V_o$ falls below $V_{\text{ref}}$.
- Circuit achieved efficiency > 70 % for a wide range of output voltages and power.

Source - Voltage Scalable Switched Capacitor DC-DC Converter for Ultra-Low-Power On-Chip Applications
GENERAL IMPLEMENTATION ON-CHIP

4. HYBRID REGULATORS

- Combination of switched capacitor circuit and linear regulators:

- Source - A Fully Integrated On-Chip DC–DC Conversion and Power Management System
Monolithic DC-DC converters are implemented in low-voltage nano-meter CMOS technologies and so these transistors cannot directly handle the higher voltages which may be applied to a buck converter on-chip. In such cases cascode-bridge circuits are used which enable higher voltages (say $nV_{\text{max}}$) to be applied directly.

Circuit for $2V_{\text{max}}$: 

![Circuit diagram](image)
INTEGRATION OF PASSIVE COMPONENTS

Reasons for integrating passives –

- Reduced system mass, volume and footprint. Individual packages are eliminated and passives can go “underground,” leaving more room on the surface for ICs.
- Improved electrical performance. Integrated passives can have lower parasitics, particularly, much lower inductance in capacitors.
- Increased design flexibility. The component’s resistance, capacitance, or inductance can be sized to any desired value within the technology’s range.
- Improved reliability. Solder joints are eliminated.
- Reduced unit cost. Integrated passives can be formed simultaneously and with very low incremental cost. Also, they are inherently lead-free.

Source – Integrated Passive Component Technology
Problems with integrating passives –

- Indecision on materials and processes. Research continues on many resistor materials and capacitor dielectrics.
- Lack of design tools, for both component sizing and system layout.
- Requires vertical integration. The same company must manufacture both substrates and passives.
- Yield issues. One bad component can lead to scrapping the entire board.
- Tolerance issues. Integrated passives cannot be presorted prior to inclusion on the board.
- Lack of standardization. The various segments of the integrated passive industry aren’t speaking the same language.
- Surface-mount technology is improving.
- Lack of costing models. It is not easy to tell when integrated passives might be more cost effective.
- Integrated passive components are limited to low power and hence are currently available only for low voltage converters.

Source – Integrated Passive Component Technology
On-Chip capacitors –

- The top-plate capacitance is due to the interconnect metal wires, and is usually very small compared to the capacitance $C$.

- The bottom-plate capacitor has area at least equal to the area of the capacitor $C$, and so it can have very significant value and effects on the circuit operation. ($\alpha = 10\%$)

- Source - Switched-capacitor dc-dc converters for low-power on-chip applications
On-chip inductors:

- Planer inductor and model –

- Expression for Q-factor –

\[
Q = \frac{\omega L_s}{R_s} \cdot \frac{R_p}{R_p + \left[ 1 + \left( \frac{\omega L_s}{R_s} \right)^2 \right] R_s} \cdot \left[ 1 - \frac{R_p^2 \left( C_s + C_p \right)}{L_s} - \omega^2 L_s \left( C_s + C_p \right) \right]
\]

= metal factor \cdot substrate loss factor \cdot self-resonance factor.

- Improving Q-factor
Two new and interesting methods to overcome the drawbacks of on-chip inductors are illustrated in this section.

- Solenoidal inductor

![Solenoidal inductor diagram]

**Fig. 4** External view of micro inductor.

<table>
<thead>
<tr>
<th>Structure</th>
<th>Specifications of micro inductor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device size</td>
<td>Solenoid</td>
</tr>
<tr>
<td>3.0 mm × 3.0 mm × 0.525 mm</td>
<td></td>
</tr>
<tr>
<td>Coil conductor material</td>
<td>Cu</td>
</tr>
<tr>
<td>60 μm</td>
<td></td>
</tr>
<tr>
<td>Coil conductor thickness</td>
<td>Ni-Zn Ferrite</td>
</tr>
<tr>
<td>136 μm</td>
<td></td>
</tr>
<tr>
<td>Number of turns</td>
<td>14</td>
</tr>
<tr>
<td>Inductance</td>
<td>1.81 μH (at 0.3 A, 2.3 MHz)</td>
</tr>
<tr>
<td>DC resistance</td>
<td>0.13Ω</td>
</tr>
<tr>
<td>AC resistance</td>
<td>2.06 Ω (at 0.3 A, 2.3 MHz)</td>
</tr>
</tbody>
</table>

**Fig. 2** External view of micro DC-DC converter module.

**Fig. 3** Cross sectional view of micro DC-DC converter module.
• Magnetic material integration:

- Insulating media
- Metal spiral
- Magnetic film

(a) Substrate

(b)

(c)

(d)

(e)

• Resulting improvements:
ADDITIONAL TOPICS

- On-chip capacitors –
  - MIM capacitors
  - Stack and comb capacitors

- Novel implementations –
  - Charge/energy recycling from parasitics
  - Intelligent load response (micro-processor load)
REFERENCES

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  - Multi-voltage CMOS Circuit Design, by Volkan Kursun and Eby G. Friedman (John Wiley and Sons Ltd.)
  - Integrated Passive Component Technology (Introduction by R.K. Ulrich downloaded from net)

- **Papers** –
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- PhD-Thesis of Vincent Lorentz, Submitted to the School of Engineering of the University Friedrich-Alexander of Erlangen-Nuremberg
Thank You